AMENDMENTS TO THE SPECIFICATION

Please amend the paragraphs beginning on page 7, line 15, and ending on page 8, line 10, with the following amended paragraphs.

A collector terminal of the IGBT 1 is connected to ~~an inverting~~ a noninverting input port of a first comparator COMP 1 via a diode D1. An anode terminal of the diode D1 and the ~~inverting~~ noninverting input port of the first comparator COMP 1 are connected to a line power voltage Vcc via a resistance Rbias. The resistance Rbias is a bias resistance for setting a conduction current value of the diode D1.

Furthermore, a first reference voltage V1 is applied to a ~~noninverting~~ an inverting input port of the first comparator COMP 1 and the first comparator COMP 1 comprises a collector voltage detection circuit for comparing the first reference voltage V1 with a collector voltage (an anode terminal voltage of the diode D1), which is applied to the ~~inverting~~ noninverting input port, to detect the collector voltage.

Furthermore, the gate terminal of the IGBT 1 is connected to ~~an inverting~~ a noninverting input port of a second comparator COMP 2, and a second reference voltage V2 is applied to ~~a~~ ~~noninverting~~ an inverting input port of the second comparator COMP 2. The second comparator COMP 2 comprises a gate voltage detection circuit for comparing the gate terminal of the IGBT with the second reference voltage V2 to detect the gate voltage.

Please amend the paragraphs beginning on page 12, lines 5 to 18, with the following amended paragraphs.

In the second embodiment, resistances R1 and R2 are connected between a gate of the IGBT and ~~an inverting~~ a noninverting input port of a second comparator COMP 2. The second embodiment is structured identically to the first embodiment except that these resistances R1, R2 are connected. Therefore, detailed description of the second embodiment is omitted.

One end of the resistance R1 is connected to the gate of the IGBT 1, the other end of the R1 being connected to ~~an inverting~~ a noninverting input port of the second comparator COMP 2. One end of the resistance R2 is connected to the other end of the resistance R1 and the ~~inverting~~ noninverting input port of the second comparator COMP 2.

The gate voltage is configured such that it is divided by these resistances R1, R2 and the divided voltage is inputted to the ~~inverting~~ noninverting input port of the second comparator COMP 2.